WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising the steps of:

forming a plurality of projected gate portions by forming a plurality of gate electrodes in a line shape in parallel on a gate oxide film formed so as to cover a main surface of a semiconductor substrate and by forming a sidewall spacer serving as an insulating film covering a side of said gate electrode;

forming an interlayer insulating film covering an upper side of said projected gate portion and a gap between said projected gate portions, with respect to said projected gate portion;

forming a contact hole reaching a first bottom portion introduced into said semiconductor substrate, from an upper surface of said interlayer insulating film through the gap between said projected gate portions;

forming a second bottom portion having said semiconductor substrate exposed on a bottom face and a side face by forming a diffusion prevention film covering a side face of said first bottom portion and by etching further a bottom face of said first bottom portion; and

forming a plug by filling said contact hole with polysilicon having an impurity doped.

2. The method of manufacturing a semiconductor device according to claim 1, wherein

said step of forming the second bottom portion by etching is performed by wet etching.

3. The method of manufacturing a semiconductor device according to claim 1, wherein

undoped polysilicon is used as said diffusion prevention film.

4. The method of manufacturing a semiconductor device according to claim 1, wherein

polysilicon doped with boron is used as said diffusion prevention film.

5. The method of manufacturing a semiconductor device according to claim 1, further comprising the step of diagonally injecting a P-type impurity onto said gate oxide film exposed between said gate electrodes prior to forming said sidewall spacer, to form a region having the P-type impurity doped so as to extend to a position directly under said gate electrode.

6. The method of manufacturing a semiconductor device according to claim 1, further comprising the step of injecting an N-type impurity onto a bottom face of said contact hole, prior to said step of forming a plug.

7. A method of manufacturing a semiconductor device, comprising the steps of:

forming a sidewall spacer covering a side of each of a plurality of gate electrodes formed in a line shape in parallel on a gate oxide film formed so as to cover a main surface of a semiconductor substrate, and forming a first bottom portion introduced into said semiconductor substrate through said gate oxide film exposed between said gate electrodes;

forming a stopper film covering an upper side of said semiconductor substrate including said first bottom portion;

forming an interlayer insulating film covering an upper side of said stopper film;

forming a contact hole reaching said stopper film from an upper surface of said interlayer insulating film through a gap between said gate electrodes;

forming a second bottom portion having said semiconductor substrate exposed on a bottom face and a side face by forming a diffusion prevention film covering a side face of said first bottom portion by partially removing said stopper film and by etching further a bottom face of said first bottom portion; and

forming a plug by filling said contact hole with polysilicon having an impurity doped.

8. The method of manufacturing a semiconductor device according to claim 7, wherein

the step of forming said second bottom portion by etching is performed by wet etching.

9. A semiconductor device, comprising:

a semiconductor substrate;

a plurality of gate electrodes formed in a line shape in parallel on said semiconductor substrate, with a gate insulating film interposed;

a plug electrode formed in a gap between said gate electrodes with polysilicon having an impurity doped, so that a lower end of the plug electrode is introduced into said semiconductor substrate; and

a diffusion prevention film extending so as to cover a side face of said plug electrode in a vicinity of the lower end of said plug electrode, and so as to be introduced into said semiconductor substrate.

10. The semiconductor device according to claim 9, further comprising a region where a P-type impurity is doped, so as to extend to a position directly under said gate electrode.

11. The semiconductor device according to claim 9, wherein

an N-type impurity is injected into a portion in contact with the lower end of said plug electrode in said semiconductor substrate.